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Y	NSMITS A		TION DISCLOSURE STA R 1.97(b) or 1.97(c))	ATEMENT	111	cket No. 0030066US1						
Re Application Of: METHODS AND APPARATUS FOR DEFECT ISOLATION.												
Applic	ation No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.						
10/708380		02/27/04	Unassigned	024241	·							
Title: 11ETHODS AND APPARATUS FOR DEFECT ISOLATION.												
Address to: Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450												
37 CFR 1.97(b)												
1. 🛚	The Information Disclosure Statement submitted herewith is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits, or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.											
	37 CFR 1.97(c)											
2.	CFR 1.97(I Final Actio	he Information Disclosure Statement submitted herewith is being filed after the period specified in 37 FR 1.97(b), provided that the Information Disclosure Statement is filed before the mailing date of a inal Action under 37 CFR 1.113, a Notice of Allowance under 37 CFR 1.311, or an Action that therwise closes prosecution in the application, and is accompanied by one of:										
the statement specified in 37 CFR 1.97(e);												
		(OR									
	☐ the f	ee set forth in 37 CF	R 1.17(p).									

TEXAL OF INFORMATION DISCLOSURE STATEMENT Docket No. (Under 37 CFR 1.97(b) or 1.97(c)) BUR920030066US1 METHODS AND APPARATUS FOR DEFECT ISOLATION. Customer No. Group Art Unit Confirmation No. Examiner Application No. Filing Date 024241 Unassigned 10/708380 02/27/04 METHODS AND APPARATUS FOR DEFECT ISOLATION. Payment of Fee (Only complete if Applicant elects to pay the fee set forth in 37 CFR 1.17(p)) is attached. A check in the amount of The Director is hereby authorized to charge and credit Deposit Account No. 09-0456 as described below. Charge the amount of Credit any overpayment. XCharge any additional fee required. Certificate of Mailing by First Class Mail Certificate of Transmission by Facsimile* I certify that this document and fee is being deposited on I certify that this document and authorization to charge deposit mail under 31 C.F.R. 1.8 and is addressed to the account is being facsimile transmitted to the United States Patent and Trademark Office (Fax. No. Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 (Date) Signature of Person Mailing Correspondence Signature Phyllis deLangis Typed or Printed Name of Person Mailing Certificate Typed or Printed Name of Person Signing Certificate *This certificate may only be used if paying by deposit account. Dated: 7/28/2004 obet A. Wall Robert A. Walsh, Esq. Reg. No.: 26,516 **IP Law Department IBM Corporation** 1000 River Street - 972E Essex Junction, VT 05452

CC:

Express Mail Label No.:

PATENTS

Docket No. BUR920030066US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

licants : Leendert M. Huisman, William V. Huott

and Franko Motika

Serial No. : 10/708,380

Filed : February 27, 2004

For : METHODS AND APPARATUS FOR DEFECT

ISOLATION

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

AUG 0 2 2004

In accordance with 37 C.F.R. §§ 1.56 and 1.97, applicants wish to call the attention of the Examiner to the following references:

E.B. Eichelberger, et al., "A Logic Design Structure for LSI Testability", Proceedings of the Fourteenth Design Automation Conference, New Orleans, 1977, pps. 462-468.

David P. Vallett, "IC Failue Analysis: The Importance of Test and Diagnostics", IEEE Design & Test of Computers, July-September 1997, pps. 76-82.

James L. Schafer et al., "Partner SRLS for Improved Shift Register Diagnostics", IEEE VLSI Test Symposium, June 1992, pps. 198-200.

Sandip Jundu, "Diagnosing Scan Chain Faults", IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 2, No. 4, December 1994, pps. 512-517.

Samantha Edirisooriya et al., "Diagnosis of Scan Path Failures", Proceedings of IEEE VLSI Test Symposium April 1995, pps. 250-255.

Sridhar Narayanan et al., "An Efficient Scheme to Diagnose Scan Chains", International Test Conference, July 1997, pps. 704-713.

These references also are listed on the accompanying Information Disclosure Statement (Form PTO-1449). The submission of this Information Disclosure Statement shall not be construed as a representation that a search has been made or that no other art than that identified above exists.

Consideration of the foregoing in relation to this patent application is respectfully requested.

Respectfully Submitted,

Brian M. Dugan d Esq. Registration No. 41,720 Dugan & Dugan, PC

Attorneys for Applicants (914) 332-9081

Dated: June 16, 2004

Tarrytown, New York

U.S	. Depar	tment of Commerc	Docket No.: BUR920030	0066US1	Serial No.: 10/708,380				
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	AJ	E.B. Eichelberger, et al, "A Logic Design Structure for LSI Testability", Proceedings of the Fourteenth Design Automation Conference, New Orleans, 1977, pps. 462-468.							
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	AL			tics", IEEE Design & Te SRLS for Improved Shif					
		June 1992, pps. 19	98-200.	•				•	
	AM		_	n Chain Faults", IEEE Tr er 1994, pps. 512-517.	ansactions On Very L	arge Scale In	tegration	(VLSI)	
	AN	; 		iagnosis of Scan Path Fa	ilures", Proceedings of	of IEEE VLSI	Test Syr	mposium Ar	
	1	1995, pps. 250-25	•	-			•	•	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

Sridhar Narayanan et al., "An Efficient Scheme to Diagnose Scan Chains", International Test Conference, July

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Examiner

1997, pps. 704-713.

Date Considered